IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

ACQIS LLC, Plaintiff, vs. ASUSTEK COMPUTER, Inc., Defendant, INVENTEC CORPORATION, Defendant, LENOVO GROUP LTD. et al, Defendants, MITAC COMPUTING TECHNOLOGY CORPORATION, Defendant, WIWYNN CORPORATION, Defendant.	§ §	Civil Action No.: 6:20-cv-965-ADA Civil Action No.: 6:20-cv-966-ADA Civil Action No.: 6:20-cv-967-ADA Civil Action No.: 6:20-cv-962-ADA Civil Action No.: 6:20-cv-968-ADA

DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF

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Exhibits 1-26 were attached to Defendants Opening Brief. Exhibits 27-34 are attached hereto.

All emphases have been added unless otherwise noted.

Defendants' claim constructions are true to the intrinsic record—the plain language of the claims, the complete disclosure of the patent specifications, and ACQIS's repeated admissions before the Patent Office to save its patents. Every part of the intrinsic record confirms that the recited PCI bus transactions are transactions in accordance with the industry standard PCI Local Bus Specification, as Defendants propose—and other Courts have agreed, including most recently in the *Samsung* case. Ex. 27 at 19. The intrinsic record also establishes that the claimed PCI bus transactions always include the control signals that ACQIS omits. The PCI Local Bus Specification expressly requires control signals to define PCI transactions—*e.g.*, when and how the transaction begins and ends. Ex. 11 at 26. And the patent specifications confirm that the same control signals are present. *See infra* Section A.4. Indeed, before the Patent Office, ACQIS's own expert admitted that control signals are required: "***they define the transaction, so have to be there.***" Ex. 12, 145:24–146:17. This is a clear and unmistakable disclaimer that is binding on ACQIS. *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353 (Fed. Cir. 2017). Thus, every part of the intrinsic record confirms that a PCI bus transaction requires more than the address, data and command information that ACQIS now urges for infringement purposes.

In an effort to obscure the clear intrinsic record, ACQIS misrepresents its *IPR* admissions, examines patent excerpts out of context, and ignores the requirements of the PCI Local Bus Specification. Rather than refute Defendants' constructions on the merits, ACQIS adds unstated requirements—*e.g.*, that every section of the PCI Local Bus Specification must be read into the claims—to attack a strawman construction. And ACQIS runs the same playbook for the "Universal Serial Bus (USB) protocol" terms to escape its prior admission that "the term 'USB' refers to the versions of the USB specification in existence at the time of the invention, including USB 2.0 and prior versions." Ex. 17 at 10. Defendants' construction tracks this statement and

Judge Payne's recent *Samsung* opinion construing the USB terms as referring to USB 2.0. Ex. 27 at 31-33. In sum, ACQIS disregards the intrinsic record to blur the distinction between (i) what a POSITA would have understood as requirements of the then-existing PCI and USB protocols of ACQIS's claims, and (ii) ACQIS's cherry-picked subset of information—*e.g.*, address and data information—which cannot of itself (without other necessary information that ACQIS discards) define the transaction or protocol recited by the claim language. For the remaining terms, ACQIS's positions also ignore the consistent teachings of the patent specifications and should be rejected.

A. "Peripheral Component Interconnect (PCI) Bus Transaction" / "PCI Bus Transaction"

ACQIS asks this Court to limit a PCI bus transaction to require only "PCI address, data, byte enable, and command type information." While ACQIS claims that its proposal "aligns with Judge Davis's prior construction" (Resp. at 7), ACQIS fails to mention that Judge Davis rejected ACQIS's attempt to limit a PCI bus transaction to a subset of information, holding that "a PCI bus transaction must include ***all*** information required by the PCI standard" and "[the PCI Local Bus Specification] ***does not clearly define a 'transaction' as digital command, address, and data information***." *EMC E.D. Tex. Markman*, 2015 WL 1737853, at *5. As demonstrated below—and as recently recognized by Judge Payne (Ex. 27 at 17-19)—the PCI Local Bus Specification and the asserted patents, especially in view of ACQIS's unequivocal disclaimers at *IPR*, do not limit a PCI bus transaction to ACQIS's infringement-driven proposal.

1. ACQIS Disclaimed Its Proposed Construction To Preserve The Validity Of Its Patents

In its Response ("Resp.") to Defendants' Opening Claim Construction Brief ("Br."), ACQIS states "[b]efore the PTAB, as here, ACQIS contended that a 'PCI bus transaction' should be construed in accordance with the ***information*** required by the PCI Specification." Resp. at 18. Not true. ACQIS told the PTAB that a PCI Bus Transaction is a ***transaction.*** *E.g.* Br. at 10-11;

Ex. 5 at 5 ("PCI Bus Transaction is properly limited to bus transactions according to the Peripheral Component Interconnect protocol."). ACQIS's unequivocal admissions that a PCI bus transaction is a transaction are binding intrinsic evidence that the Court must hold ACQIS to. *See e.g.*, *Aylus Networks, Inc.*, 856 F.3d at 1361-62.

ACQIS also made clear and unmistakable statements to the PTAB that a PCI bus transaction requires control signals. Br. at 17-18. ***First***, ACQIS's *IPR* expert Dr. Lindenstruth admitted that a PCI bus transaction requires control signals. *Id.* ACQIS attempts to dismiss Dr. Lindenstruth's irrefutable testimony by claiming that "when read as a whole (rather than the selective cherry picking done by Defendants), the testimony . . . is consistent with a 'transaction' not including the control signals themselves." Resp. at 19. In fact, Dr. Lindenstruth's testimony read "as a whole" says the opposite. Ex. 12 at 142:4-146:17. ACQIS cites a single paragraph of Dr. Lindenstruth's declaration to argue that he did not admit a PCI bus transaction requires control signals. Resp. at 20. EMC's counsel directed Dr. Lindenstruth to that same paragraph and asked him if control signals are "also part of what the claims require as a PCI bus transaction." Ex. 12 at 145:18-146:17. He unequivocally said yes:

> Q. Do these ***control lines, such as frame, target ready, and so forth***, are they part of the PCI bus transaction as you understand that term in the claims of the patent?
>
> MR. DAVIS: Objection; form.
>
> Q. So, you know, earlier we were talking about what your understanding of the term "PCI bus transaction", ***looking at paragraph 114***, for example, of your declaration, and you stated claims require address and data phases of a PCI bus transaction, et cetera. ***Are these control lines also part of what the claims require as a PCI bus transaction***?
>
> A. Since they are required to define what is going on on the bus at any point in time, ***the answer is yes***. ***They define the PCI transaction.*** If you, for example, would remove from one byte enable you have no way of knowing whether we are reading,

> writing, or what other functionality is to be executed. If you remove any of the flow control signals, you cannot steer the fact if a device is not immediately ready, which happens a lot. So they would have to be -- ***they define the transaction, so have to be there.***

Id. Dr. Lindenstruth makes clear that control signals are required to ***define*** the transaction—*e.g.*, the beginning and end of a transaction. ACQIS's allegation that a POSITA would read his testimony as ambiguous or subject to more than one reasonable interpretation is incredible.

Second, ACQIS's counsel also repeatedly told the PTAB that a PCI bus transaction according to the PCI Local Bus Specification requires control bits. Br. at 18, 23. ACQIS argues that despite saying "***control*** bits," counsel was actually referring to command information. Resp. at 18-20. However, the PCI Local Bus Specification distinguishes "control" from "command." *See, e.g.*, Ex. 11 at 10 (describing "***command***" signal C/BE[3::0]# and "***control***" signals FRAME#, IRDY#, TRDY#). And the '873 patent at issue at *IPR* could not be more clear: "A specific example of a ***control signal*** is ***FRAME#*** used in PCI buses. ***A control bit*** . . . ***is a data bit that represents a control signal.***" '873 patent, 17:30-32. Even assuming the veracity of ACQIS's *post hoc* explanation, its counsel said "control bits" and the public is entitled to rely on those admissions. *See Tech. Props. Ltd. LLC v. Huawei Techs. Co.*, 849 F.3d 1349, 1359 (Fed. Cir. 2017) ("But the scope of surrender is not limited to what is absolutely necessary to avoid a prior art reference; patentees may surrender more than necessary. When this happens, we hold patentees to the actual arguments made, not the arguments that could have been made.") ACQIS's counsel's statements that control bits are required, viewed with its expert's unequivocal admission that control signals are "part of what the claims require as a PCI bus transaction," inform a POSITA that the claimed PCI bus transaction must include control signals. *See id.* ("The question is what a [POSITA] would understand the patentee to have disclaimed during prosecution, not what . . . the patentee needed to disclaim during prosecution.").

2. The Legal Conclusion Of ACQIS's IPR Admissions Is That ACQIS Is Bound To Its Disclaimers

As a matter of law, ACQIS is bound by its IPR admissions that a PCI bus transaction includes control signals. *E.g.*, *Biogen Idec, Inc. v. GlaxoSmithKline LLC*, 713 F.3d 1090, 1095 (Fed. Cir. 2013). ACQIS argues that requiring control signals would improperly exclude preferred embodiments of the patents. Resp. at 1, 6, 8, 14. As explained in Section A.4 below, that is not true, the patents require control signals as part of a PCI bus transaction. But even if that were true, "[w]hen a patentee has disavowed a claim scope that would cover embodiments disclosed in the specification, there is no legal requirement the disavowed claim be construed to embrace such embodiments." *nCAP Licensing, LLC v. Apple Inc.*, No. 2:17-cv-905, 2019 WL 2409666, at *6 (D. Utah June 7, 2019); *see also N. Am. Container, Inc. v. Plastipak Packaging, Inc.*, 415 F.3d 1335, 1346 (Fed. Cir. 2005) ("[L]imitations may be construed to exclude a preferred embodiment if the prosecution history compels such a result.").

ACQIS further argues that its disclaiming statements regarding the '873 and '814 patents cannot attach to the Reissue Patents because the Reissue Patents do not claim priority to either of the *IPR* patents. Resp. at 30, n. 11. But "the prosecution history regarding a particular limitation in one patent is presumed to inform the later use of that same limitation in ***related patents***[.]" *Trading Techs. Int'l, Inc. v. Open E Cry, LLC*, 728 F.3d 1309, 1323 (Fed. Cir. 2013). The Reissue Patents and the Non-Reissue patents are related—both purport to incorporate by reference the same provisional application, and ACQIS cites to that provisional for written support. *E.g.*, Ex. 28 at 5, 30; Ex. 29 at 4, 41. And ACQIS itself concedes that the "the disclosures of the [the Reissue Patents] overlap substantially with the [Non-Reissue Patents]" and the differences in specifications of the Non-Reissue and Reissue patents "do not suggest any different interpretation of a 'PCI bus transaction.'" Resp. at 4, 10 n. 7.

3. The PCI Local Bus Specification Does Not Limit A PCI Bus Transaction To ACQIS's Subset Of Information

The PCI Local Bus Specification is ***intrinsic*** evidence that demonstrates a PCI bus transaction requires more than the subset of information ACQIS identifies. Br. 14-16. As Defendants explained, the Specification teaches that a PCI bus transaction requires address and data phases, control signals, and parity. *Id.* For example, Figure 3-5 (shown right) of the Specification "illustrates a read transaction." Ex. 11 at 47. It depicts not only address (AD) and command/byte enable (C/BE#) signals, but also control signals FRAME#, IRDY#, TRDY#, and DEVSEL#. Citing Figure 3-5, the Specification states: "The fundamentals of ***all PCI data transfers*** are controlled with three signals . . . FRAME# . . . IRDY# . . . TRDY#." Ex. 30 at 26. The Specification further explains how each control signal is used during a transaction. For example, the Specification states that FRAME# "indicate[s] the ***beginning and end of a transaction***" (*id.*), and it explains that "a read transaction [] starts with ***an address phase which occurs when FRAME# is asserted for the first time***[.]" Ex. 11 at 47.[1]

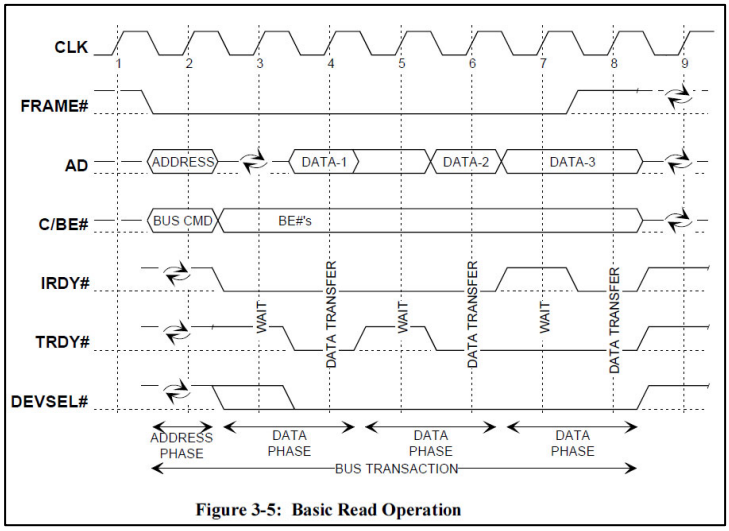

Figure 3-5: Basic Read Operation

ACQIS concedes that the PCI Local Bus Specification defines a "transaction" as an "address phase plus one or more data phases," but argues the claims require only some information transmitted during those phases. Resp. at 12-13, 18. In particular, ACQIS argues that a POSITA reading the patents and the Specification would understand that the control signals are not required.

[1] *See also* Ex. 11, at 49 ("All transactions are concluded when FRAME# and IRDY# are both deasserted, indicating an Idle state."); *id.* at 301 ("All transactions are concluded when FRAME# and IRDY# are deasserted (an idle cycle).")

Id. at 13. But ACQIS's own *IPR* expert, Dr. Lindenstruth, agreed that control signals are "also part of what the claims require as a PCI bus transaction," and explained that they "have to be there [because] they define the transaction." Ex. 12, 145:17-146:17; *see also* Ex. 32 at ¶¶ 19, 25.[2]

Defendants also explained that the PCI Local Bus Specification teaches that a PCI bus transaction requires parity signals. Br. at 15-16. ACQIS's arguments to the contrary are contradictory and wrong. First, ACQIS argues that parity is not part of a PCI bus transaction because it is sent "after the 'transaction'" itself. Resp. at 13. Not so. Parity signals "lags the corresponding address or data by one clock"; they are not delayed until a transaction is complete. *See* Ex. 11 at 94, Fig. 3-20. Indeed, ACQIS later concedes parity is calculated during a transaction. Resp. at 17 ("[P]arity is calculated on a 'transaction' during a 'transaction[.]'") (emphasis modified). That the Specification at one point describes calculating parity "*on* all PCI transactions" is not, as ACQIS contends, proof that parity is not part of a transaction. *Id.* Elsewhere the Specification describes Figure 3-20 as "illustrat[ing] both read and write transactions ***with*** parity." Ex. 11 at 94. ACQIS's semantics aside, it is undisputed that "parity generation is not optional" and that it "provides a mechanism to determine for each transaction if the master is successful in addressing the desired target and if data transfers correctly between them." *Id.* That is, parity is a required element of a PCI bus transaction that ensures each stage of a transaction successfully occurs. *See* Ex. 32 at ¶¶ 13-15, 25.[3]

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[2] In its Response, ACQIS relies extensively on the declarations of Dr. Marc E. Levitt, submitted in support of ACQIS's claim construction briefing in another case, *ACQIS LLC v. Samsung Elec. Co., Ltd., et al.*, No. 2:20-cv-00295-JRG. To rebut that extrinsic evidence, Defendants have cited to the expert declarations of Dr. Robert Colwell, submitted in support of Samsung's claim construction briefing. Exs. 31, 32.

[3] ACQIS also argues that its constructions are consistent with the purported purpose of the invention to provide an interface that is compatible with legacy PCI communications (Resp. at 1-2, 6, 10-12, 14, 34, 36-37), yet its infringement-driven constructions would prevent backward

4. The Patent Specifications Do Not Limit A PCI Bus Transaction To ACQIS's Subset Of Information

ACQIS argues the patent specifications support limiting a PCI bus transaction to only "PCI address, data, byte enable, and command type information." Resp. 9-11. They do not. ACQIS relies primarily on Figure 13 of the Non-Reissue patents (annotated below), and includes an annotated version in its Response. But the patent specifications teach that the two CK+ columns that ACQIS failed to highlight (outlined in blue) are bits (BS0-BS3) that represent "part of the function of ***PCI control signals***, such as FRAME#, IRDY#, and TRDY#." '873 patent, 20:44-47. Though ACQIS concedes that BSO-BS3 may "represent PCI control signals," ACQIS contends that is limited to only some embodiments. Resp. at 17. But one of the disclosures ACQIS dismisses as just "one embodiment" is the same disclosure that ACQIS relies on to argue a PCI bus transaction requires "address bits," "data bits," and, "byte enable information bits." *Compare* Resp. at 17 (citing '768 patent, 21:37-58) *with* Resp. at 10 (same). And ACQIS fails to address that the Non-Reissue specifications state that "***in the present invention***"—with no limitation to a specific embodiment—"PCI control signals are encoded into control bits and the control bits . . . are transmitted on the interface channel." *E.g.*, '873 patent, 5:33–36; *see Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) ("When a patent . . . describes the features of the 'present invention' as a whole, this description limits the scope of the invention."). As ACQIS concedes, the Reissue Patents do not contain Fig. 13 and its corresponding disclosures

Chu Fig. 13, illustrating PCI address information, data information, byte enable information, and command information

PCK	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-
PD0	BS0	CM0#	A00	A01	A02	A03	A04	A05	A06	A07	BS0	BE0#	D00	D01	D02	D03	D04	D05	D06	D07
PD1	BS1	CM1#	A08	A09	A10	A11	A12	A13	A14	A15	BS1	BE1#	D08	D09	D10	D11	D12	D13	D14	D15
PD2	BS2	CM2#	A16	A17	A18	A19	A20	A21	A22	A23	BS2	BE2#	D16	D17	D18	D19	D20	D21	D22	D23
PD3	BS3	CM3#	A24	A25	A26	A27	A28	A29	A30	A31	BS3	BE3#	D24	D25	D26	D27	D28	D29	D30	D31
PCN	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9

compatibility because they do not account for all of the information required by a PCI bus transaction in the legacy PCI Local Bus Specification.

that ACQIS says show encoded PCI control signals are optional. Resp. at 10, n. 7. But the Reissue Patents do describe encoding PCI control signals into control bits and transmitting them on the interface channel, untethered to "one embodiment." *E.g.*, '140 patent, 17:24-30. Thus, the specifications of both the Non-Reissue and Reissue patents describe a PCI bus transaction that includes control bits representing PCI control signals. *See also* Ex. 32 at ¶¶ 20-26.

5. Defendants' Proposal Will Resolve The PCI Claims

ACQIS asserts that Defendants' proposed construction "lacks sufficient detail to resolve any dispute" because it is either (1) overbroad or (2) insufficiently clear.[4] Resp. 13-15. It is neither. Defendants propose the same construction that resolved the *EMC* case. Br. at 6-7. ACQIS tries to escape that fact by arguing that the *EMC* court "altered" the claim construction of "PCI Bus Transaction" at summary judgment. Resp. 14. But the record shows ACQIS, not the *EMC* court, tried to modify the court's construction at summary judgment to resurrect its infringement case. *EMC D. Mass. Summary Judgment*, 2021 WL 1088207, at *4 ("All of ACQIS's arguments are attempts to skirt the claim construction set forth by Judge Davis and this Court . . . Put simply, ACQIS is attempting to reopen claim construction."); *id.* at *5 ("The Court rejects ACQIS's proffered modification of the claim term 'PCI bus transaction' to narrow the application and meaning of the Specification."). In any event, ACQIS's complaints that the *EMC* court modified its construction of a PCI bus transaction to require "every element" of the PCI Specification are overstated. Resp. at 14, 21. The *EMC* court granted summary judgment based on a set of narrow, undisputed facts: ACQIS did not dispute EMC's products did not include "an address phase followed by one or more data phases as well as control signals and parity signals." *EMC D. Mass.*

[4] By ACQIS's logic, its construction is just as unclear. That a PCI bus transaction includes "at least" certain information does not provide an upper bound for the content of a signal that would qualify as a PCI bus transaction.

Summary Judgment, 2021 WL 1088207, at *4. And those are the same elements Defendants say a PCI bus transaction requires here. Br. at 14-16.[5]

6. Collateral Estoppel Applies, And ACQIS's Arguments In Opposition Are Legally and Factually Wrong

Defendants explained that collateral estoppel bars ACQIS from advancing its proposed construction for both "PCI bus transaction" and claims that recite specifics "bits" of a "PCI bus transaction." Br. at 19-20, 25-26. ACQIS's arguments to the contrary do not overcome that bar. ***First***, ACQIS argues that the *EMC* court relied solely on agreed constructions and therefore did not consider the intrinsic evidence. Resp. at 20, 25. Not true. For "PCI bus transaction," Judge Burrough's construction and grant of summary judgment were based on Judge Davis' holding that "a PCI bus transaction must include all information required by the PCI standard" and his rejection of ACQIS's attempt to "define a 'transaction' as digital command, address, and data information." *EMC D. Mass Summary Judgment*, 2021 WL 1088207, at *3-4 ("This Court, together with Judge Davis, has fulfilled the first part of the infringement analysis through the claim construction process . . . All of ACQIS's arguments are attempts to skirt the claim construction set forth by Judge Davis and this Court."); *EMC E.D. Tex. Markman*, 2015 WL 1737853, at *5. For the "specific bits" terms, Judge Burroughs adopted the parties' construction because it "is also supported by the intrinsic evidence." *EMC D. Mass. Markman*, 2017 WL 6211051, at *8.[6]

[5] ACQIS also argues that because the PCI "specification relates to many things other than just 'transactions,'" a construction that references the Specification without more is "absurd." Resp. at 14-15. But Defendants' proposal states "a ***transaction*** in accordance with the industry standard PCI Local Bus Specification . . ." No POSITA would understand ***a transaction*** to require all of the physical and electrical disclosures in the Specification, which ACQIS concedes are "things other than just 'transactions.'" Resp. at 14; *see also* Ex. 32 at ¶ 9; Ex. 31 at ¶ 58.

[6] These excerpts also defeat ACQIS's claim that the *EMC* court "did not address the merits of ACQIS's arguments regarding the proper scope of the parties' stipulated construction, and thus the issue was not actually litigated." Resp. at 22-23.

Second, ACQIS argues that there is no collateral estoppel because an appeal is pending. Resp. at 22. ACQIS is mistaken. The regional circuit's collateral estoppel rules govern. *See Novartis Pharm. Corp. v. Watson Labs., Inc.*, 611 Fed. Appx. 988, 997 (Fed. Cir. 2015). In the Fifth Circuit, "the finality of a judgment is not affected by the pendency of an appeal." *Welch v. All Am. Check Cashing, Inc.*, No. 3:13-cv-271, 2015 WL 4066495, at *5 (S.D. Miss. July 2, 2015) (collecting cases).[7]

Third, ***ACQIS*** argues the *EMC* court's ruling should not apply because the claims and disclosures here are different from those there. Resp. at 23. For example, ACQIS says the *EMC* court did not address claim language reciting only certain bits, like "address and data bits of a Peripheral Component Interconnect (PCI) bus transaction." *Id.* But the *EMC* case involved nearly identical language. *See* Ex. 14 at 21 (showing exemplary claim language at issue included "address and data bits of PCI bus transaction" (RE 42,814, claims 24 and 31)). And ACQIS's argument that the *EMC* court did not address embodiments without a PCI bus is misleading given that the *EMC* court agreed with ACQIS and expressly held a PCI bus transaction does ***not*** require a PCI bus. *EMC D. Mass. Markman*, 2017 WL 6211051, at *4.[8]

B. Claims Reciting Specific "Bits" of a PCI Bus Transaction

As Defendants explained, "ACQIS's *IPR* counsel and expert unequivocally admitted at *IPR* that claims that recite ***only specific bits*** of a PCI bus transaction ***still*** require 'a PCI bus transaction, including all address, data, and control bits.'" Br. at 22-25. Those admissions, which form binding disclaimers now, recognize that you cannot have the claimed PCI bus transaction

[7] *See also Wright v. Transportation Commc'n Union/IAM*, No. 4:20-cv-0975, 2020 WL 7061874, at *3 (S.D. Tex. Nov. 5, 2020), *adopted*, 2020 WL 7060213 (S.D. Tex. Dec. 1, 2020) ("The Fifth Circuit has established that, for purposes of collateral estoppel, a judgment may be final even though an appeal is pending.").

[8] The patents at issue in *EMC* did contain the embodiment shown in Fig. 8B. RE42,984, Fig. 20.

without the other required elements of the transaction. Yet, ACQIS's construction attempts to read out a "PCI bus transaction" from the claims. ACQIS does not substantively address Defendants' argument. Instead, ACQIS argues that Defendants' construction is wrong because it (1) ignores express claim language; (2) violates the presumption of claim differentiation; and (3) conflicts with the specifications' disclosures. Resp. at 24-25. But, as Defendants explained and ACQIS did not attempt to rebut, all of those principles are trumped by ACQIS's *IPR* disclaimers.

First, ACQIS's allegation that "Defendants never address the difference in scope between claims that recite specific bits of a 'PCI bus transaction' and claims that do not" is wrong. Defendants explained that the *EMC IPRs* involved both claims that recited a PCI bus transaction (*e.g.*, '873 patent, claim 54) and claims that recite specific bits of a PCI bus transaction (*e.g.*, '873 patent, claim 61). Br. at 23-24. Defendants explained "that claim 61 recited specific bits of a PCI bus transaction—while other claims did not—was a central issue in dispute at the *IPR*." *Id.* at 24. And Defendants explained that ACQIS's counsel and expert unequivocally admitted that a PCI bus transaction requires control bits whether or not the claim recites specific bits of a PCI bus transaction. Br. at 24-25. For example, Dr. Lindenstruth explained that despite claim 24 of the '814 patent "explicitly" reciting only "address and data bits," it still required any "other corollary information which is needed to define a PCI transaction." Ex. 12 at 121:13–17. Later, Dr. Lindenstruth explained that the PCI control signals were also "corollary signals which basically define what's going on[.]" *Id.* at 142:17–143:8. Thus, Defendants addressed the difference in scope of the claims, but ACQIS chose not to address those arguments.[9]

[9] The *Samsung* court declined to hold ACQIS to its counsel's disclaiming statements. Ex. 27 at 22-23. But the court was not directed to Dr. Lindenstruth's unequivocal admission that even a claim reciting "address and data bits of [a] PCI bus transaction" still requires "other corollary information which is needed to define a PCI transaction." Ex. 12 at 121:13-17.

Second, ACQIS's allegation that Defendants' construction violates the presumption of claim differentiation is belied by its *IPR* admissions that it ignores. As Defendants explained, EMC argued that the doctrine of claim differentiation meant that the scope of the PCI bus transaction of claims 54 and 61 were different because claim 61 recited "address and data bits" while claim 54 did not. Br. at 23-24; Ex. 4 at 14:20-21. ACQIS opposed EMC's claim differentiation argument regarding claim 61, explaining that the only difference between claim 54 and claim 61 was that claim 61 carved out "interrupt acknowledgements," not control bits. Ex. 4 at 35:11–24. ACQIS does not address those statements.

Third, ACQIS's argument that Defendants' proposed construction conflicts with the specifications' disclosures also misses the mark. The specifications consistently describe PCI bus transactions compliant with the PCI Local Bus Specification requiring more than address, data and byte enable bits. *See supra* Section A.4. Regardless, a patentee can disclaim even a preferred embodiment. *N. Am. Container*, 415 F.3d at 1346; *nCAP Licensing*, 2019 WL 2409666, at *6.

C. Claims Reciting an "Encoded" PCI Bus Transaction or a PCI Bus Transaction in "Serial Stream" or "Serial Form"

All of the claims associated with these terms recite a "PCI bus transaction." *See Ex.* 15. It is undisputed that a PCI bus is a ***parallel*** bus. *E.g.*, Resp. at 1 (describing prior art "parallel Peripheral Component Interconnect (PCI) bus"). ACQIS's purported invention, on the other hand, is a ***serial*** bus. *Id.* What the specifications describe and ACQIS argued at *IPR*, yet denies now, is that the claims require serializing the otherwise parallel PCI bus transactions, irrespective of whether the claims recite a PCI bus. The Court should adopt Defendants' construction, which holds ACQIS to its past statements and patent teachings.

ACQIS cannot deny that to preserve the validity of the '873 patent that it asserts here, it argued that "[a]s described in the specification . . . ***one key to the invention was to serialize the***

otherwise parallel PCI bus transactions[.]"). Ex. 3 at 3. Nor that it argued that prior art failed to describe "serializ[ing] an actual PCI bus transaction." *Id.* at 21-22. Nor can ACQIS deny that its counsel told the Board that "the whole point" of the invention was "I'm going from parallel, I'm putting on a serial line." Ex. 4 at 30:13-31:2. Finally, ACQIS cannot deny that those statements, and others (Br. 28-29), led Judge Burroughs to find that "an encoded PCI transaction requires that a PCI bus transaction be encoded for serial transmission from a parallel form." *EMC D. Mass. Markman*, 2017 WL 6211051, at *7. Instead, ACQIS argues that the court should reject the *EMC* construction and give "greater weight" to Judge Davis' previous construction of "encoded PCI bus transaction" because it "was legally determined by the court rather than stipulated to by the parties, was used in a jury trial, and was not disturbed on appeal." Resp. at 27, 32. Apart from ACQIS's incorrect suggestion that the parties "stipulated" to the encoded construction in *EMC*, ACQIS's argument glosses over a key issue: Judge Davis' construction predated ACQIS's unequivocal *IPR* admissions that the Court now must account for.

ACQIS further argues that the Court should ignore ACQIS's *IPR* disclaimers and the *EMC* construction because, according to ACQIS, *some* of the asserted patents (but not the '873, '624, and '984 patents which also recite "encoded . . ." terms) include additional figures (8A, 8B) that are not present in the *EMC IPR* patents. Resp. at 30, 33.[10] ACQIS argues those figures' disclosures of a chip directly connected to a serial interface with no parallel interface (*i.e.*, a PCI bus) directly contradict ACQIS's *IPR* statements that parallel-to-serial is required. *Id.* But that argument is inconsistent with what ACQIS is ***currently*** arguing before the PTAB. Several pending *IPR* petitions allege that ACQIS did not properly incorporate by reference Figures 8A and 8B (which originally appear in U.S. Prov. Appl. No. 60/086,886 ("Chu '886")) until 2011, when ACQIS filed

[10] ACQIS omits that the patents in *EMC* did include Figs. 8A, 8B. *See* RE42,984, Figs. 19, 20.

application no. 13/087,912. *E.g.*, Ex. 33 at 36-37. In rebuttal, ACQIS admits that Figures 8A and 8B come from Chu '886 (Ex. 28 at 8) and argues that "***every patent*** in the '768 patent's priority chain properly incorporated Chu '886 by reference through Chu '330." Ex. 28 at 30; *see also id.* at 5 ("Chu '330 and Chu '886 are part of the disclosure of ***each application*** in the priority chain[.]") The '873 patent is in that priority chain. Ex. 2. Therefore, according to ACQIS and inconsistent with its Response, the '873 patent includes Figures 8A and 8B.[11]

Moreover, ACQIS fails to mention that it advanced essentially the same argument, and lost, before the *EMC* court. *EMC D. Mass Markman*, 2017 WL 6211051, at *5 ("ACQIS suggests that because several of the claims describe communicating encoded PCI bus transactions '***without an intervening PCI bus***,' parallel-to-serial conversion must not be required."). ACQIS lost because it told the PTAB that parallel-to-serial conversion is required even when ***"there's no PCI bus."*** Ex. 4 at 46 (explaining that despite Figure 8 of the '873 patent showing "no PCI bus" and "the claims don't require a bus," the claims still "require a PCI transaction to take place" that involves "***taking it at a parallel form, putting it into serial form and then back to parallel***."). ACQIS's counsel was right—no matter the hardware configuration, the claimed PCI bus transaction ***is a parallel transaction***. Ex. 32 at ¶ 32. To transmit a parallel transaction across a serial interface requires the parallel transaction be serialized. *Id.* at ¶¶ 30-37.

Defendants explained that the patent specifications support its proposed construction. Br. at 29-32. ACQIS argues that Defendants are wrong because Figure 10 of the '873 patent shows

[11] The *Samsung* court did not apply ACQIS's disclaiming statements in that case because the '873 patent "has a different disclosure and claim set." Ex. 27 at 26. However, the '873 patent *is* asserted here, and the parties failed to inform the court of ACQIS's *IPR* statements regarding Figures 8A and 8B, which contradict the *Samsung* court's finding that "the '873 Patent does not include anything equivalent to Figures 8A and 8B of the '768 Patent." Additionally, the court's reasoning that "the claims of the Asserted Patents do not require a PCI bus transaction at all" is not applicable here because ***all*** of the "encoded" terms requires a PCI bus transaction. *See* Ex. 15.

encoding as a separate process from the serial-parallel converters. Resp. at 28. But as ACQIS acknowledges, the encoders of Fig. 10 "format the PCI address/data bits to a form more suitable ***for parallel to serial conversion***[.]" '873 patent, 16:55-58. That conversion occurs ***before*** the address/data bits are "transmitt[ed] on the XP Bus," *i.e.* the serial interface. *Id.* Thus, the claims at issue here that recite encoded PCI bus transactions ***on a serial interface*** involve transactions converted from parallel. Therefore, Figure 10 supports Defendants' proposed construction.

D. "Universal Serial Bus (USB) protocol"

As Defendants' construction makes clear (and the recent *Samsung* decision confirms (Ex. 27 at 31-33), the USB protocol terms are properly construed with reference to the USB 2.0 Specification—the version of the protocol existing at the time of the patent application filing. The USB 2.0 Specification is intrinsic evidence on the face of the patents, and it is how a POSITA would understand what the USB protocol terms require.

ACQIS concedes (as it must) that the claims refer to version 2.0 (and earlier) of the USB specifications (Resp. at 38), but then attacks strawman positions that Defendants' constructions do not require—*i.e.*, that the terms require a "Universal Serial ***Bus***" or "all aspects of the USB specifications." Resp. at 35. What Defendants contend, and the USB 2.0 Specification makes clear, is that the USB protocol requires more than communicating some ***data*** or ***information***. That could occur under ***any*** protocol. And nothing in the intrinsic record justifies ignoring the plain meaning of the USB protocol terms to require just data or some arbitrary subset of the USB protocol. For example, ACQIS argues that USB "data" refers to information described in the USB specification as the "data payload." As Defendants explained, the USB ***protocol*** requires more than a data payload, that is, more than the data portion of a transaction. Br. at 35-37. The USB 2.0 Specification explains that the "protocol" is a "specific set of rules, procedures, or conventions relating to ***format and timing of data transmission*** between two devices." Ex. 20 at 8.

ACQIS also argues that Defendants have mischaracterized its position with regard to the later generation USB 3.0 specification. Not so. Making what appears to be infringement-related arguments (Resp. at 36-38), ACQIS contends—without a single reference to the intrinsic record—that USB 3.0, which did not exist at the time of the patent filing, somehow comes within the scope of a proper claim construction. That is misleading at best. As the *Samsung* court stated, the term "Universal Serial Bus (USB) protocol" must be interpreted as of the priority date. Ex. 27 at 32-33. This Court should likewise reject ACQIS's efforts to shoehorn into its claims a version of the USB protocol that did not exist at the time of the patent filing. Moreover, it is ACQIS that mischaracterizes Defendants' position—Defendants ***never agreed*** that a communication channel can satisfy both USB 2.0 and USB 3.0 at the same time. Resp. at 37. Nor does (or could) ACQIS point to any such admission by Defendants. Contrary to ACQIS's bare assertions, there are substantial differences between USB 2.0 and USB 3.0, and most importantly for claim construction, USB 3.0 comes too late. Ex. 31 at ¶¶ 60-63; Ex. 32 at ¶¶ 43-45.

ACQIS further misstates Defendants' position on "data packets" in an attempt to disguise its unsupportable position that the term "USB protocol" simply refers to a USB data payload. Resp. at 38-39. ACQIS does not dispute that some of the asserted claims recite "***Universal Serial Bus (USB) protocol*** data packets" or "data packets in accordance with a ***Universal Serial Bus (USB) protocol***."[12] But ACQIS fails to address that under its construction those terms would have the following nonsensical interpretations: "[USB data payload] packets" and "data packets in accordance with a [USB data payload]." Defendants' arguments merely point out ACQIS's attempt to confuse a USB data packet with a USB data payload. Moreover, as the USB 2.0 Specification makes clear, a USB 2.0 transaction has three elements: a "token packet," a

[12] '750 patent, claims 4, 7, 24, 46; '359 patent, claims 1, 6, 19; '977 patent, claim 1.

"handshake packet," and a "data packet," and the data packet includes more than its data payload. Br. at 37; Ex. 20 at 8. In short, the terms reciting "USB protocol" (or "USB protocol data") do not merely refer to a USB data payload, as ACQIS proposes.

E. "Computer Module"

ACQIS argues that (1) Defendants' construction improperly imports elements into the term "computer module," and (2) Defendants' use of the terms "user-removable, user-portable" introduces ambiguity that is likely to confuse the jury. Resp. at 39-43. ACQIS is wrong.

First, Defendants' construction, unlike ACQIS's, is directly supported by all relevant intrinsic evidence. Br. at 38-40. Every embodiment in the patent specifications discloses a "computer module" that consists of an enclosure that is insertable into and removable from a console that houses at least a processor, memory, and mass storage. *Id.* There is ***no*** embodiment in which a computer module does not include these generic "computer components." '768 Patent 9:56. Yet, ACQIS argues that two claims of the '873 and '624 patents suggest that a computer module does not require a mass storage device. Resp. at 41. That argument contradicts the Abstract and the "Brief Summary of the Invention" of the '873 and '624 patents which state that "[e]ach of the computer modules has . . . a mass storage device." *E.g.*, '873 patent, Abstract, 4:24-28, 39-43. Nonetheless, Defendants are willing to omit "mass storage" device from their proposed construction to resolve this dispute, and bring Defendants' construction in line with what ACQIS advanced in a different case concerning related patents, where it argued that a "computer module" was "an assembly" comprising "at least a processing unit[] [and] memory." *See* Ex. 34 at 11-12. In contrast to Defendants' intrinsic-based construction, ACQIS's proposed construction is unsupported and vague. The specifications do not use the terms "computing package" or "computing function," or set forth what those terms are intended to mean. "[C]laims cannot be of broader scope than the invention that is set forth in the specification." *On Demand Mach. Corp.*

v. Ingram Indus., Inc., 442 F.3d 1331, 1340 (Fed. Cir. 2006). And those terms are so broad that they are meaningless in this context. The Court should thus reject ACQIS's construction.

Second, ACQIS's assertion that the terms "user-removable" and "user-portable" would be confusing to a jury strains credibility. There is nothing about the concepts of removability or portability—which the specifications describe as the advantages of the claimed computer modules (*e.g.*, '768 patent, 2:14-55)—that would be confusing to jurors, as mobile computing devices are ubiquitous today. Indeed, Judge Davis held "the patents' consistent emphasis that a module is '***removable***' warrants including that limitation in the claim construction." *EMC E.D. Tex. Markman*, 2015 WL 1737853, at *6.[13] ACQIS distorts the meaning of a single specification excerpt to incorrectly argue that the computer modules need not be portable or removable. Resp. at 41. But that portion of the specification ('768 patent at 1:43-48) supports Defendants' proposed construction, stating that the present invention relates to portable or modular computing, whether applied to a desktop or to a server.

Finally, ACQIS argues that "nothing in the specification" limits the portability or removability to a "user." Resp. at 42. This argument, however, ignores Defendants' discussion of the specifications' express statements regarding the invention. The specifications describe that the claimed "computer module" addressed a problem that desktop computers were not fit for use "on the road"—*i.e.*, were not "portable." Br. at 39. Such portable use can only be achieved with a "computer module" that is removable by the user. Requiring an IT professional or other technician with adequate tools and training to remove the computer module, as ACQIS suggests, would not allow for work "on the go" and would therefore not address this portability problem.

[13] Judge Davis's finding there that "user-portable" "introduces unnecessary ambiguity" into the construction is incorrect as the term "portable" appears throughout the specifications of the Asserted Patents and is a readily-understood word. *E.g.*, '768 patent, 2:14-55.

Indeed, the '654 patent specification states that the modular computer may be located at a home ('654 Patent 9:56-10:3), where IT professionals would not assist with removal.[14]

F. "Console"

Defendants' construction of "console" is supported by the intrinsic evidence (Br. at 41-42), whereas ACQIS's is not. ACQIS incorrectly contends that the '768 patent "makes clear that 'the console is an enclosure capable of housing each coupling site.'" Resp. at 43. In fact, the very same passage of the specification ACQIS relies on expressly defines a "coupling site" to be a "computer module bay." '768 patent, 4:33. Moreover, none of the Reissue Patents' specifications or claims recite the term "coupling site." Thus, to the extent ACQIS asserts a "coupling site" is not a "computer module bay," this assertion improperly excludes all the embodiments in the Reissue Patents. Defendants' construction is consistent with ***all*** embodiments of the inventions and the express language of the claims in ***all*** the Asserted Patents.

ACQIS's inclusion of "device" in its proposed construction has no support. The word "device" serves only to broaden the clams unjustifiably, as a "device" can be almost anything, whereas an "enclosure" has a specific, understood meaning. Indeed, previously ACQIS argued that a "console" was "***a chassis*** that connects several components of the computer system," and opposed a construction of "***a device*** that supplies a module with a primary input, display, and power supply to form an operating computer system." *See EMC E.D. Tex. Markman*, 2015 WL 1737853, at *7. Likewise, ACQIS argued that the term "console" means "***an enclosure*** with internal power and data connections for housing computer modules and other computer system

[14] ACQIS also misrepresents Defendants' brief as saying "'many of the alleged inventive embodiments' describe the computer module as being removable." Resp. at 41. Defendants' brief instead describes (i) how the problem all embodiments attempted to solve was to create a portable computer that had the performance of a desktop, (ii) an important aspect of this portability is that a user can easily remove it from a console, and (iii) that this removability is described in the discussion of many of the disclosed embodiments. Br. at 39-40.

components to the extent recited in the claims." *See* Ex. 34 at 16-17 ("The Patents-in-Suit uniformly teach that a console is a peripheral 'enclosure'[.]"). ACQIS's argument that because the specifications describe that a console in one instance may be "a chassis and a motherboard" and therefore can be a "device" and not just an "enclosure" is nonsensical. Resp. at 43. The fact that a chassis—which is an enclosure—might have a motherboard within it does not make it a device. There is no basis to add the word "device" to the construction of the term "console."[15]

G. "Single Chip"

Defendants' construction resolves the dispute between the parties as to the ordinary meaning of this term. In every instance, the Asserted Patents use the term "chip" to refer to an integrated circuit chip.[16] When a patentee uses a claim term throughout the entire patent specification in a manner consistent with only a single meaning, he has defined that term "by implication." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582, 1584 n.6 (Fed. Cir. 1996). Integrating one integrated circuit chip with another integrated circuit chip creates two integrated circuit chips, not the "single chip" recited in the claims.

H. "Central Processing Unit"

Defendants' construction is consistent with how a person of ordinary skill in the art would understand the term "central processing unit" and should be adopted. Defendants' proposed construction distinguishes instances where Dual-CPU systems are described in the patent specifications from the claimed single CPU systems. *See, e.g.*, '768 patent 2:62-3:17; '873 patent 2:51-3:5.

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[15] The *Samsung* construction of "console" that includes "a device" was based on the parties' agreement which, as explained here, is unsupported by the intrinsic evidence. Ex. 27 at 34.

[16] *See, e.g.*, '768 patent 1:49-52, 7:7-13, 11:27-38, 16:29-31, 26:10-14 & Fig. 8B; '654 patent 1:41-44, 6:51-61, 14:34-46, 15:10-14.

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CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and Local Rule CV-5, I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served with a copy of the foregoing document via the Court's CM/ECF system on October 1, 2021.

/s/ Christopher Kao
Christopher Kao